**Digital Logic Design (DLD)**

**(Lab Task No 4)**



Session (2022-2026)

Program

**BS-Computer Science**

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**EXPERIMENT 04:**

**Implementation of a Half Adder and a Full Adder using gates. Implementation of 4-bit Adder and Subtractor using 74LS83 & 74LS86.**

**Objectives:**

To implement a half adder and a full adder using gates and implementing 4-bit adder and subtractor using 74LS83 & 74LS86.

**Equipment/Tool:**

Trainer, IC – XOR, IC-OR, IC-AND, IC74LS83 (4-bit adder), 74LS86 (XOR).

**Background theory:**

A half adder is a combinational circuit that adds two binary inputs. It gives two outputs, S as the sum and C as the carry of the inputs. A full adder is a combinational circuit that adds three binary inputs X, Y and Z. The input Z is the carry input from another addition. It gives two outputs, S as the sum and C as the carry of the inputs.

The circuit for the adder/subtractor shown in figure 4.3 is used to do binary additions and subtractions. If Cin=0, addition is performed and if Cin=1, subtraction is performed.

**Tasks:**

* Write a truth table for a half adder, design a simplified circuit for it. Implement it on trainer and verify the results.
* Write a truth table for a full adder, design a simplified circuit for it. Implement it on trainer and verify the results.
* Fill in the truth table.
* Design the complete circuit on the trainer and verify the results.

**Procedure**

**Task 1 & 2**

Fill in the following truth table of half adder and full adder and draw the circuit from

**HALF ADDER**

**ANSWER:**

**Table for Half Adder:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **Sum** | **Carry** | **Proof Circuits** |
| 0 | 0 | 0 | 0 |  |
| 0 | 1 | 1 | 0 |  |
| 1 | 0 | 1 | 0 |  |
| 1 | 1 | 0 | 1 |  |

**FULL ADDER**

**ANSWER:**

**Table for Full Adder:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **Sum** | **Carry** | **Proof Circuits** |
| 0 | 0 | 0 | 0 | 0 |  |
| 0 | 0 | 1 | 1 | 0 |  |
| 0 | 1 | 0 | 1 | 0 |  |
| 0 | 1 | 1 | 0 | 1 |  |
| 1 | 0 | 0 | 1 | 0 |  |
| 1 | 0 | 1 | 0 | 1 |  |
| 1 | 1 | 0 | 0 | 1 |  |
| 1 | 1 | 1 | 1 | 1 |  |

**Implementation of 4-bit Adder and Subtractor using 74LS83 & 74LS86.**

**Exercise in Lab:**

Fill in the following truth table, verify your results, and show it to the instructor:-

|  |  |  |  |
| --- | --- | --- | --- |
| A3 | A2 | A1 | A0 |
|  |  |  |  |
| B3 | B2 | B1 | B0 |
|  |  |  |  |
| S3 | S2 | S1 | S0 |
|  |  |  |  |

**Answer:**

|  |  |  |  |
| --- | --- | --- | --- |
| A3 | A2 | A1 | A0 |
| 1 | 0 | 1 | 0 |
| B3 | B2 | B1 | B0 |
| 0 | 1 | 0 | 1 |
| S3 | S2 | S1 | S0 |
| 1 | 1 | 1 | 1 |

**Verification:**

